FORM PTO-1390 (Modified) (REV 11-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)
112740-253	09/889649

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/EP00/00326	14 January 2000	19 January 1999

TITLE OF INVENTION

METHOD FOR THE TIME SYNCHRONIZATION OF A COMPUTER NETWORK, AND COMPUTER NETWORK WITH TIME SYNCHRONIZATION

APPLICANT(S) FOR DO/EO/US

Richard Sturm et al.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210).
8. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. ☒ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☒ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☒ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☒ Certificate of Mailing by Express Mail
20. ☒ Other items or information:

Submission of Drawings FIgures 1-2 on two sheets

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/889649	PCT/EP00/00326	112740-253

21. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐	Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO	$1,000.00
☒	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but Internation Search Report prepared by the EPO or JPO	$860.00
☐	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO	$710.00
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4)	$690.00
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4)	$100.00

ENTER APPROPRIATE BASIC FEE AMOUNT =		$860.00
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).		$0.00

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	16 - 20 =	0	x $18.00	$0.00
Independent claims	2 - 3 =	0	x $80.00	$0.00
Multiple Dependent Claims **(check if applicable)**.			☐	$0.00

☐	**TOTAL OF ABOVE CALCULATIONS =**	$860.00
☐	Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) **(check if applicable).**	$0.00
	SUBTOTAL =	$860.00
☐	Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +	$0.00
☐	**TOTAL NATIONAL FEE =**	$860.00
☐	Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).**	$0.00
☐	**TOTAL FEES ENCLOSED =**	$860.00
	Amount to be: refunded	$
	charged	$

☒ A check in the amount of **$860.00** to cover the above fees is enclosed.

☐ Please charge my Deposit Account No. in the amount of to cover the above fees.
A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **02-1818** A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

William E. Vaughan (Reg. No. 39,056)
Bell, Boyd & Lloyd LLC
P.O. Box 1135
Chicago, Illinois 60690

SIGNATURE

William E. Vaughan
NAME

39,056
REGISTRATION NUMBER

July 19, 2001
DATE

BOX PCT

IN THE UNITED STATES ELECTED/DESIGNATED OFFICE
OF THE UNITED STATES PATENT AND TRADEMARK OFFICE
UNDER THE PATENT COOPERATION TREATY-CHAPTER II

SUBMISSION OF DRAWINGS

APPLICANTS:	Richard Sturm et al.l.	DOCKET NO: 112740-253
SERIAL NO:		GROUP ART UNIT:
		EXAMINER:
INTERNATIONAL APPLICATION NO:		PCT/EP00/00326
INTERNATIONAL FILING DATE:		14 January 2000
INVENTION:	METHOD FOR THE TIME SYNCHRONIZATION OF A COMPUTER NETWORK, AND COMPUTER NETWORK WITH TIME SYNCHRONIZATION	

Assistant Commissioner for Patents,
Washington, D.C. 20231

Sir:

Applicants herewith submit two sheets (Figs. 1-2) of drawings for the above-referenced PCT application.

Respectfully submitted,

(Reg. No. 39,056)

William E. Vaughan
Bell, Boyd & Lloyd LLC
P.O. Box 1135
Chicago, Illinois 60690-1135
(312) 807-4292
Attorneys for Applicants

Fig. 1

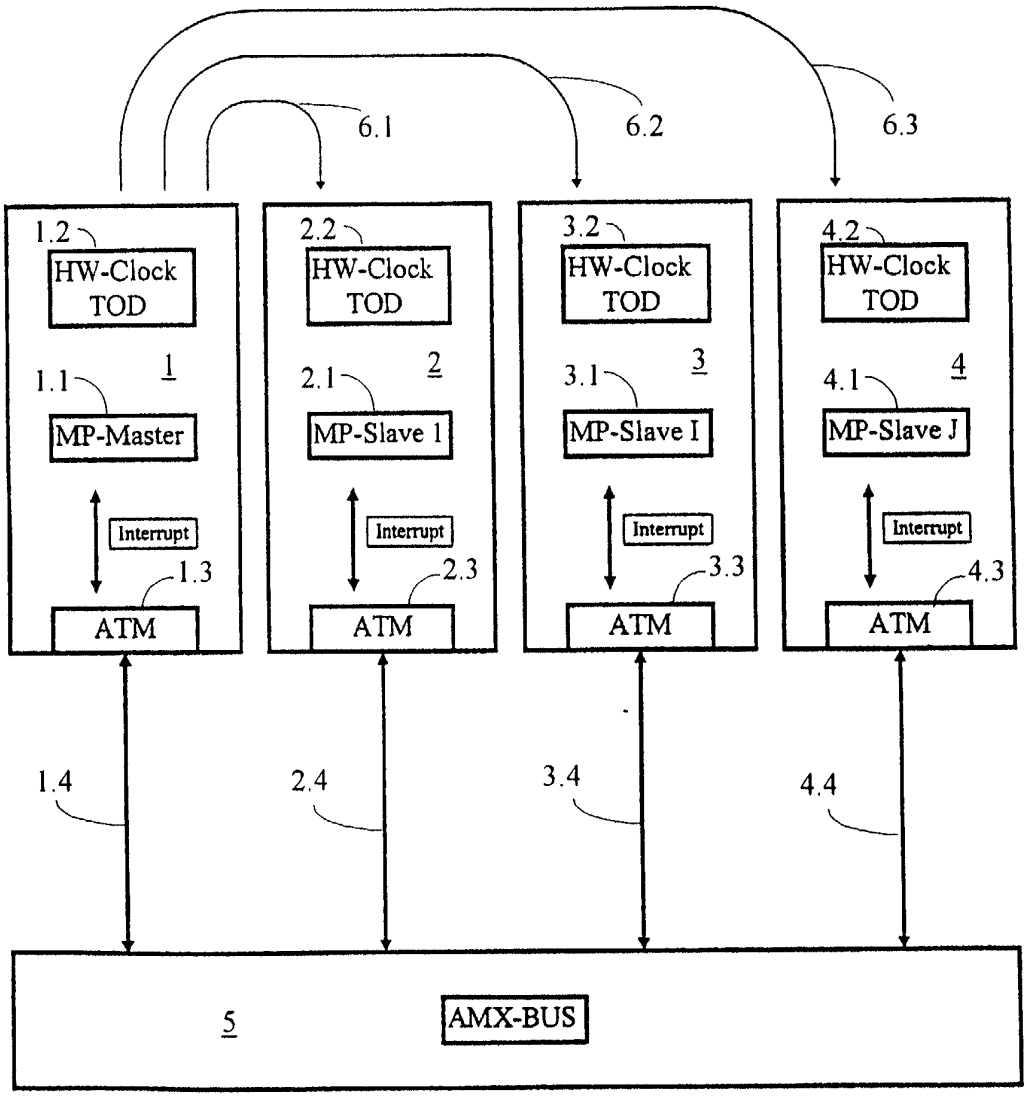
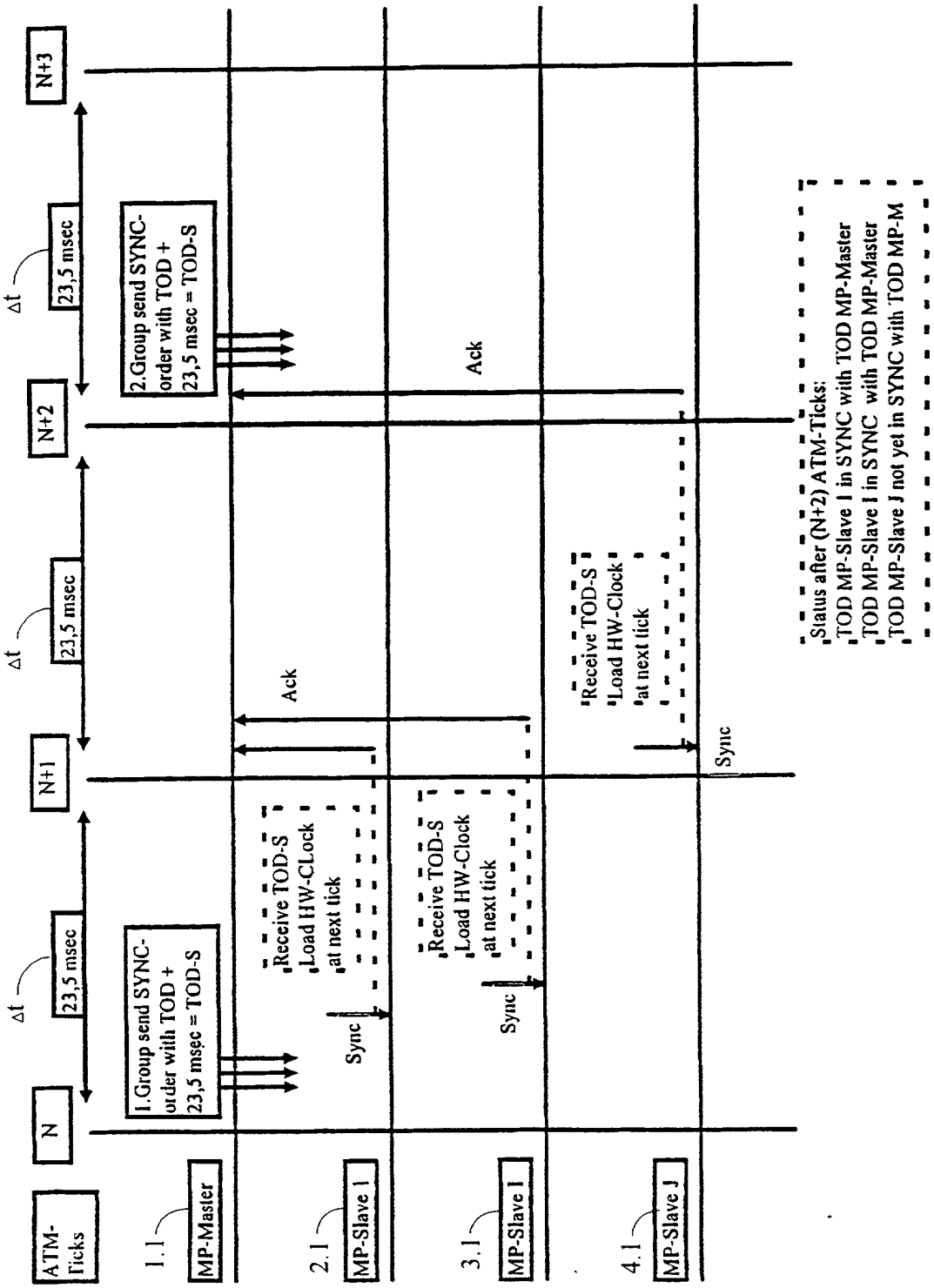

6.1
6.2
6.3
1.2
HW-Clock TOD
1
1.1
MP-Master
Interrupt
1.3
ATM
2.2
HW-Clock TOD
2
2.1
MP-Slave 1
Interrupt
2.3
ATM
3.2
HW-Clock TOD
3
3.1
MP-Slave I
Interrupt
3.3
ATM
4.2
HW-Clock TOD
4
4.1
MP-Slave J
Interrupt
4.3
ATM
1.4
2.4
3.4
4.4
5
AMX-BUS

Fig. 2



BOX PCT

IN THE UNITED STATES ELECTED/DESIGNATED OFFICE
OF THE UNITED STATES PATENT AND TRADEMARK OFFICE
UNDER THE PATENT COOPERATION TREATY-CHAPTER II

PRELIMINARY AMENDMENT

APPLICANTS:	Richard Sturm et al..	DOCKET NO: 112740-253
SERIAL NO:		GROUP ART UNIT:
		EXAMINER:
INTERNATIONAL APPLICATION NO:		PCT/EP00/00326
INTERNATIONAL FILING DATE:		14 January 2000
INVENTION:	METHOD FOR THE TIME SYNCHRONIZATION OF A COMPUTER NETWORK, AND COMPUTER NETWORK WITH TIME SYNCHRONIZATION	

Assistant Commissioner for Patents,
Washington, D.C. 20231

Sir:

Please amend the above-identified International Application before entry into the National stage before the U.S. Patent and Trademark Office under 35 U.S.C. §371 as follows:

In the Specification:

Please replace the Specification of the present application, including the Abstract, with the following Substitute Specification:

SPECIFICATION

TITLE

METHOD FOR THE TIME SYNCHRONIZATION OF A COMPUTER NETWORK, AND COMPUTER NETWORK WITH TIME SYNCHRONIZATION

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a method for time synchronization of a computer network, preferably of a switching computer system, including at least one main computer (Master) with, in each case, at least one assigned secondary computer (slave), each computer being provided with at least one internal clock, and the computers being connected via at least one ATM bus (ATM = asynchronous transfer mode).

Furthermore, the present invention relates to a computer network, preferably a switching computer system, including at least one main computer (Master) with, in each case, at least one assigned secondary computer (Slave), each computer being provided with at least one internal clock, and the computers being interconnected via at least one ATM bus.

Description of the Prior Art

At present there is no known prior art for real-time process computer systems, particularly switching computer systems, in which time synchronization of the participating computers in the computer network is achieved with an accuracy with regard to date and time of day of at least +/- 50 msec and a relative time stamp of at least +/- 1 msec. The currently used switching computer systems such as, for example, the applicant's switching computer system EWSD or EWSX, are achieved either as mono-processor systems or strictly coupled multi-processor systems. With this type of configuration, particular time synchronization is inherently given on account of the strict coupling of the processors, or of the just one processor that is present.

In the course of general development, however, distributed real-time process computer systems are also intended to be used as switching computer systems. The requirement for charge registration necessitates the process computers situated in the process computer system to be provided with a synchronized time, with regard to date and time of day, which has a maximum error of +/- 50 msec. This requirement is substantiated by the charge registration since the charge registration creates tickets with a time indication at all the computer components of the distributed system. Furthermore, it is necessary, on account of the internal data

transport protocol of the distributed system, to achieve a relative time stamp, or a counter, with an accuracy of at least +/- 1 msec for all the computers in the network system. The relative resolution of such a time stamp, that is to say the time spacing from one counter to the next counter, typically lies in a range of about 10 msec. The time stamp is required in order to measure message throughput times in the system, so as to analyze incorrect behavior or to carry out performance analyses in the distributed system, with the aid of system tracers. In order for the events from the trace results to be correctly assigned with respect to time, a system-wide synchronized time of day, that is to say a correspondingly exact time stamp, is likewise required.

It is an object of the present invention, therefore, to present a method for time synchronization of a computer network, preferably of a switching computer system, and a corresponding computer network, preferably a corresponding switching computer system, which achieves time synchronization for date/time of day of at least +/- 50 msec and for a general relative time stamp of at least +/- 1 msec, using no direct connection between the individual computers, but rather only the ATM bus.

SUMMARY OF THE INVENTION

With regard to the present invention's method for time synchronization of a computer network, preferably of a switching computer system, including at least one main computer (Master) and, in each case, at least one assigned secondary computer (Slave), each computer being provided with at least one internal clock, and the computers being connected via at least one ATM bus (ATM = asynchronous transfer mode), at least the following method steps are proposed:

- the at least one main computer transmits, with an N-th interrupt of a sequence of interrupts which are transmitted at a fixed time interval Δt, via the ATM bus a synchronization message (Sync) with a time indication (TOD), the time indication corresponding to the time of the main computer at the instant of the N-th interrupt plus the time interval Δt;

- the at least one secondary computer reads, with good probability, the synchronization message via the ATM bus, sets its internal clock to the communicated time with the occurrence of the next interrupt and transmits, via the ATM bus, a success message (Ack) with an identifier of the secondary computer to the main computer;

- the main computer reads the success message and decides, on the basis of the message propagation time, whether the success message was transmitted at the right time;

- in the case of correctly timed transmission, the corresponding secondary computer is defined as synchronized; and

- in the case of non-correctly timed transmission, the corresponding secondary computer is defined as unsynchronized.

In accordance with an alternative embodiment of the method according to the present invention, there may also occur between the interrupts outlined above further interrupts which are not taken into account in the method for time synchronization.

In accordance with the concept of the present invention, the main computer, with the (N + 2)-th interrupt, can again carry out time synchronization in accordance with the abovementioned method in order for secondary computers that were possibly non-synchronized during the first scan through the time synchronization to be synchronized via the renewed performance of the time synchronization. Moreover, after a certain period of time has elapsed, differences in running of the individual hardware clocks of the individual computers of the computer network can give rise to a relative deviation in the timekeeping of the individual computers, thereby necessitating renewed synchronization.

It goes without saying that these time synchronizations can be repeated at specific predetermined intervals in order to keep the computer network permanently time-synchronized.

In accordance with the method according to the present invention, an identification mechanism for synchronized or non-synchronized computers can be

established in the main computer, in which a specific secondary computer is deemed to be synchronized if the success message arrives at the main computer between the (N + 1)-th and the (N + 2)-th interrupt.

In this way, the main computer (in each case, without setting up any other particular connections to the secondary computers) can identify which secondary computers are in the synchronized state or in the non-synchronized state.

A typical magnitude of the time interval Δt at which the synchronization interrupts are transmitted is 23.5 msec. The typical accuracy of the time interval Δt is better than a few nsec, on which, however, the pure program run time, which lies in the region of a few μsec, is superposed.

A further embodiment according to the present invention involves further main computers being provided in the computer network which, in turn, have a superordinate computer, at least with regard to the system time, and are synchronized with one another according to the abovementioned method. This makes it possible for even a relatively large computer network having, for example, a number of clusters, each including a main computer and a plurality of subordinate secondary computers, to be synchronized in such a way that the main computers are first synchronized with regard to their system time and then in turn they independently synchronize, in accordance with the abovementioned method their assigned secondary computers.

However, it should be pointed out that it is also possible, in a computer network in which all the computers are interconnected via an ATM bus, to define a single main computer which carries out the time synchronization via the ATM bus, so that all, that is to say all further main computers and all secondary computers, are synchronized with this time synchronization message. If a main computer which does not itself trigger the time synchronization wishes to identify whether its secondary computers assigned to it are now time-synchronized, then it is possible for it to monitor the ATM bus with regard to the success messages of the individual secondary computers and, accordingly, to decide whether or not the secondary computers assigned to it are time-synchronized.

Advantageously, the communicated time may also include the date and, in a particular embodiment, the ATM bus may be an AMX bus.

In addition to the method of the present invention, it is proposed, in accordance with a further concept of the present invention, to configure a computer network known per se, preferably of a switching computer system, including at least one main computer (Master) with, in each case, at least one assigned secondary computer (Slave), each computer being provided with at least one internal clock, and the computers being connected via at least one ATM bus (ATM = asynchronous transfer mode), to the effect that:

- the at least one main computer is provided with a transmitter which transmits, with an N-th interrupt of a sequence of interrupts which are transmitted at a fixed time interval Δt, via the ATM bus a synchronization message (Sync) with a time indication (TOD), the time indication corresponding to the time of day of the main computer at the instant of the N-th interrupt plus the time interval Δt;
- the at least one secondary computer is provided with a part for reading the synchronization message via the ATM bus, its internal clock being set to the communicated time with the occurrence of the next interrupt, and has a transmitter for transmitting a success message (Ack) with an identifier of the secondary computer to the main computer via the ATM bus;
- the main computer has a part for reading the success message and is provided with a decision part which, on the basis of the message propagation time, decides whether the success message was transmitted at the right time;
- in the main computer a memory is provided in which there is stored, in the case of correctly timed transmission, the definition of the corresponding secondary computer as synchronized; and
- in the case of non-correctly timed transmission, the definition of the corresponding secondary computer as unsynchronized.

According to the present invention, there may also be provided, in addition to the interrupts provided for the time synchronization, further interrupts which are not taken into account during the time synchronization.

In a particular embodiment of the computer network, it may furthermore be provided that the main computer include a repetition function which, with the (N + 2)-th interrupt, again performs the time synchronization. This is particularly important if the time synchronization is intended to be maintained over a relatively long period of time.

In accordance with a particular embodiment of the inventive computer network, it is proposed that the decision part of the main computer defines a specific secondary computer as synchronized if the success message arrives at the main computer between the (N + 1)-th and the (N + 2)-th interrupt. A typical magnitude of the time interval between the interrupts may be specified as 23.5 msec.

In accordance with the method outlined above, further main computers may also be provided in the computer network, which, in turn, have a superordinate computer, at least with regard to the system time, and are synchronized with one another according to the abovementioned method.

Furthermore, it may be advantageous if the communicated time contains not only just the time of day but also the date.

In another embodiment of the computer network of the present invention, the ATM bus may be an AMX bus.

Additional features and advantages of the present invention are described in, and will be apparent from, the following Detailed Description of the Preferred Embodiments and the Drawings.

DESCRIPTION OF THE DRAWINGS

Figure1 shows schematic illustration of a computer network; abd

Figure 2 shows an illustration of the method sequence according to the present invention against the time axis.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 shows a schematic illustration of a computer network having four computers 1 to 4 illustrated by way of example. The computer 1 represents the main computer (Master) 1, which is provided with a processor (MP-Master = Main

Processor Master) 1.1, a crystal-controlled clock (HW-Clock = Hardware Clock) 1.2 and an interface 1.3 to an AMX bus 5 via the ATM connecting line 1.4.

Also shown are the secondary computers 2 to 3, which are each likewise equipped with a processor 2.1 to 4.1, a clock 2.2 to 4.2 and an ATM interface 2.3 to 4.3. The secondary computers 2 to 4 are also, in each case, connected to the AMX bus 5 via an ATM connecting line 2.4 to 4.4.

The connecting arrows 6.1 to 6.3 are intended to illustrate that the time synchronization to be carried out acts on the secondary computers 2 to 4 in a manner proceeding from the main computer 1.

Figure 2 shows the time profile of the present invention's method for time synchronization, which can be carried out using the computer network from Figure 1. The time axis t is shown running from left to right. The four computers with their processors 1.1 to 4.1 are listed in a manner arranged from top to bottom. The time synchronization interrupts (ATM ticks) are specified in the topmost line along the time axis, the interrupts having the interrupts N to N + 3 at a time interval Δt of 23.5 msec. With the first interrupt N, the main computer 1 sends a synchronization message with the current time TOD at the instant of the N-th interrupt plus 23.5 msec (TOD-S). This sent time TOD-S thus corresponds to the instant at which the (N + 1)-th interrupt occurs. In the time profile, the synchronization message (Sync) is read both at the secondary computer 2 and at the secondary computer 3. After receiving this synchronization message, the two computers 2 and 3 set their internal clocks 2.2 and 3.2 to the communicated time TOD-S with start beginning at the (N + 1)-th interrupt. In addition, after the (N + 1)-th interrupt, they send a success message (Ack) to the main computer 1 with the information that the synchronization message was received and the time on the internal clock was set correspondingly. However, the third secondary computer 4 receives the synchronization message only after the (N + 1)-th interrupt, with the result that it sets its internal clock to the communicated time only for the next interrupt; that is, for an interrupt that is too late. Consequently, its system time has an error of

$\Delta t = 23.5$ msec. Accordingly, it also sends the success message to the main computer only after the (N + 2)-th interrupt.

Thus, between the (N - 1)-th and the (N + 2)-th interrupt, the main computer registers that the two secondary computers 2 and 3 have synchronized their internal clocks 2.2 and 3.2, in accordance with the synchronization message (Sync), while no success message (Ack) has yet been transmitted by the secondary computer 3. Consequently, the main computer knows that only the secondary computers 2 and 3 have been correctly synchronized with regard to their time setting, while the fate of the computer 3 remains open. Once the main computer receives the success message of the secondary computer 3 after the (N + 2)-th interrupt, the main computer knows that this computer was definitely not synchronized correctly. With the (N + 2)-th interrupt, or in the case of the next even-numbered interrupt, the main computer once again sends a second group of synchronization messages with the current time at the instant of the (N + 2)-th interrupt plus 23.5 msec to the non-synchronized secondary computer 4 of the computer network and the synchronization of the secondary computer 4 with the subsequent signaling to the main computer starts from the beginning. In addition, the following cycles may be used to synchronize other as yet unsynchronized computers (not illustrated here).

If this method is repeated often enough, all the secondary computers are time-synchronized with the main computer. In this case, the inaccuracy of the time setting does not depend on the time profile of the message from the main computer to the secondary computer, but rather is merely dependent on the accuracy of the time interval Δt between the individual interrupts. Since the uncertainty of this time interval lies in the region of a few nsec, the time synchronization via the method described above is also extremely accurate and, thus, at any rate corresponds to the requirements of +/- 50 msec with regard to the communicated time of day including date.

If, in addition to the sent time of day, a time stamp (that is to say, a counter) is also sent with the synchronization message, the resolution of which time stamp is in the region of a few milliseconds, then the method described above also makes it

possible to set the relative time stamp of the computers of the entire computer network with an accuracy lying in the region of the resolution of the time stamp.

Consequently, the method described satisfies the requirements with regard to the synchronization time (date/time of day: +/- 50 msec, relative time stamp: +/- 1 msec).

Although the present invention has been described with reference to specific embodiments, those of skill in the art will recognize that changes may be made thereto without departing from the spirit and scope of the invention as set forth in the hereafter appended claims.

ABSTRACT OF THE DISCLOSURE

A method for-time synchronization of a computer network by a main computer, in which case, for synchronization with an N-th interrupt, a time signal corresponding to the instant of the interrupt plus a time interval between the interrupts is transmitted on an ATM bus and the secondary computers to be synchronized set their clock to this transmitted time signal with the next

In the claims:

On page 12, cancel line 1, and substitute the following left-hand justified heading therefor:

We Claim as Our Invention:

Please cancel claims 1-16, without prejudice, and substitute the following claims therefor:

17. A method for time synchronization of a switching computer system having at least one main computer with, in each case, at least one assigned secondary computer, each main and secondary computer being respectively provided with at least one internal clock and being connected via at least one ATM bus, the method comprising the steps of:

transmitting, via the at least one main computer and along the ATM bus, with an N-th interrupt of a sequence of interrupts which are transmitted at a fixed time interval, a synchronization message with a time indication and, if appropriate,

a time stamp, the time indication corresponding to a time of day of the main computer at an instant of the N-th interrupt plus the fixed time interval;

reading, via the at least one secondary computer and with good probability, the synchronization message via the ATM bus;

setting, via the at least one secondary computer, the internal clock of the at least one secondary computer to the communicated time indication upon the occurrence of the next interrupt;

transmitting, via the at least one secondary computer and along the ATM bus, a success message with an identifier of the secondary computer to the main computer;

reading, via the main computer, the success message;

deciding, via the main computer, based on a message propagation time, whether the success message was transmitted at a proper time;

defining, in the case of correctly timed transmission, the corresponding secondary computer as synchronized; and

defining, in the case of non-correctly timed transmission, the corresponding secondary computer as unsynchronized.

18. A method for time synchronization of a switching computer system as claimed in claim 17, wherein, between the interrupts of the sequence of interrupts, further interrupts can occur which are not taken into account in the time synchronization method.

19. A method for time synchronization of a switching computer system as claimed in claim 17, wherein the main computer, with the (N + 2)-th interrupt, again performs the time synchronization method.

20. A method for time synchronization of a switching computer system as claimed in claim 17, wherein a specific secondary computer is defined as

synchronized if the success message arrives at the main computer between the (N + 1)-th and the (N + 2)-th interrupt.

21. A method for time synchronization of a switching computer system as claimed in claim 17, wherein the time interval is 23.5 msec.

22. A method for time synchronization of a switching computer system as claimed in claim 17, wherein the switching computer system includes further main computers which, in turn, have a superordinate computer at least with regard to system time, the further main computers being synchronized with one another as with the main and secondary computers.

23. A method for time synchronization of a switching computer system as claimed in claim 17, wherein the communicated time indication also contains a date.

24. A method for time synchronization of a switching computer system as claimed in claim 17, wherein the ATM bus is an AMX bus.

25. A switching computer system, comprising:

at least one main computer having at least one internal clock;

at least one secondary computer having at least one internal clock, the at least one secondary computer being assigned with at least one main computer;

at least one ATM bus connecting the main and secondary computers;

when the at least one main computer transmits, with an N-th interrupt of a sequence of interrupts which are transmitted at a fixed time interval, via the ATM bus, a synchronization message with a time indication and, if appropriate, a time stamp, the time indication corresponding to a time of day of the main computer at the instant of the N-th interrupt plus the fixed time interval;

wherein the at least one secondary computer reads the synchronization message via the ATM bus, its respective internal clock being set to the communicated time indication upon the occurrence of a next interrupt of the sequence, and transmits a success message with an identifier of the secondary computer to the main computer via the ATM bus;

wherein the main computer reads the success message and decides, based on a message propagation time, whether the success message was transmitted at a proper time;

wherein, in the case of correctly timed transmission, a definition of the corresponding secondary computer as synchronized is stored in a memory of the main computer;

and wherein, in the case of non-correctly timed transmission, a definition of the corresponding secondary computer as unsynchronized is stored in the memory.

26. A switching computer system as claimed in claim 25, wherein between the interrupts of the sequence of interrupts, further interrupts can occur which are not taken into account in time synchronization.

27. A switching computer system as claimed in claim 25, wherein the main computer includes a repetition part which, with the (N+2)-th interrupt, again performs time synchronization.

28. A switching computer system as claimed in claim 25, wherein the main computer defines a specific secondary computer as synchronized if the success message arrives at the main computer between the (N+1)-th and the (N+2)-th interrupt.

29. A switching computer system as claimed in claim 25, wherein the fixed time interval is 23.5 msec.

30. A switching computer system as claimed in claim 25, further comprising:

further main computers which, in turn, have a superordinate computer at least with regard to system time, the further main computers being synchronized with one another as with the main and secondary computers.

31. A switching computer system as claimed in claim 25, wherein the communicated time indication also contains a date.

32. A switching computer system as claimed in claim 25, wherein the ATM bus is an AMX bus.

REMARKS

The present amendment makes editorial changes and corrects typographical errors in the specification, which includes the Abstract, in order to conform the specification to the requirements of United States Patent Practice. No new matter is added thereby. Attached hereto is a marked-up version of the changes made to the specification by the present amendment. The attached page is captioned "**Version With Markings To Show Changes Made**".

In addition, the present amendment cancels original claims 1-16 in favor of new claims 17-32. Claims 17-32 have been presented solely because the revisions by red-lining and underlining which would have been necessary in claims 1-16 in order to present those claims in accordance with preferred United States Patent Practice would have been too extensive, and thus would have been too burdensome. The present amendment is intended for clarification purposes only and not for substantial reasons related to patentability pursuant to 35 USC §§103, 102, 103 or 112. Indeed, the cancellation of claims 1-16 does not constitute an intent on the part of the Applicants to surrender any of the subject matter of claims 1-16.

Early consideration on the merits is respectfully requested.

Respectfully submitted,

(Reg. No. 39,056)

William E. Vaughan
Bell, Boyd & Lloyd LLC
P.O. Box 1135
Chicago, Illinois 60690-1135
(312) 807-4292
Attorneys for Applicants

VERSIONS WITH MARKINGS TO SHOW CHANGES MADE

In The Specification:

The Specification of the present application, including the Abstract, has been amended as follows:

SPECIFICATION

TITLE

~~**Method for time synchronization of a computer network, and computer network with time synchronization**~~

METHOD FOR TIME SYNCHRONIZATION OF A COMPUTER NETWORK, AND COMPUTER NETWORK WITH TIME SYNCHRONIZATION

BACKGROUND OF THE INVENTION

~~Description~~

Field of the Invention

The present invention relates to a method for ~~the~~ time synchronization of a computer network, preferably of a switching computer system, ~~comprising~~ including at least one main computer (Master) with, in each case, at least one assigned secondary computer (slave), each computer being provided with at least one internal clock, and the computers being connected via at least one ATM bus (ATM = asynchronous transfer mode).

Furthermore, the present invention relates to a computer network, preferably a switching computer system, ~~comprising~~ including at least one main computer (Master) with, in each case, at least one assigned secondary computer (Slave), each computer being provided with at least one internal clock, and the computers being interconnected via at least one ATM bus.

Description of the Prior Art

At present there is no known prior art for real-time process computer systems, ~~in particular~~ particularly switching computer systems, in which time synchronization of the participating computers in the computer network is ~~realized~~ achieved with an accuracy with regard to date and time of day of at least +/-

50 msec and a relative time stamp of at least +/- 1 msec. The currently used switching computer systems~~,~~ such as, for example, the applicant's switching computer system EWSD or EWSX, are ~~realized~~ achieved either as mono-processor systems or strictly coupled multi-processor systems. With this type of configuration, particular time synchronization is inherently given on account of the strict coupling of the processors, or of the just one processor that is present.

In the course of general development, however, distributed real-time process computer systems are also intended to be used as switching computer systems. The requirement for charge registration ~~means that it is necessary for~~ necessitates the process computers situated in the process computer system to be provided with a synchronized time, with regard to date and time of day, which has a maximum error of +/- 50 msec. This requirement is substantiated by the charge registration since the charge registration creates tickets with a time indication at all the computer components of the distributed system. Furthermore, it is necessary, on account of the internal data transport protocol of the distributed system, to achieve a relative time stamp, ~~that is to say~~ or a counter, with an accuracy of at least +/- 1 msec for all the computers in the network system. The relative resolution of such a time stamp, that is to say the time spacing from one counter to the next counter, typically lies in a range of about 10 msec. The time stamp is required in order to measure message throughput times in the system, ~~in order~~ so as to analyze incorrect behavior or to carry out performance analyses in the distributed system, with the aid of system tracers. In order ~~that~~ for the events from the trace results ~~can~~ to be correctly assigned with respect to time, a system-wide synchronized time of day, that is to say a correspondingly exact time stamp, is likewise required.

It is an object of the present invention, therefore, to present a method for ~~the~~ time synchronization of a computer network, preferably of a switching computer system, and a corresponding computer network, preferably a corresponding switching computer system, which achieves time synchronization for date/time of day of at least +/- 50 msec and for a general relative time stamp of at least +/-

1 msec, using no direct connection between the individual computers, but rather only the ATM bus ~~being utilized~~.

SUMMARY OF THE INVENTION

~~This object is achieved by means of the features of the respective first method claim and of the first apparatus claim.~~

With regard to the present invention's method for ~~the~~ time synchronization of a computer network, preferably of a switching computer system, ~~comprising~~ including at least one main computer (Master) and, in each case, at least one assigned secondary computer (Slave), each computer being provided with at least one internal clock, and the computers being connected via at least one ATM bus (ATM = asynchronous transfer mode), ~~the inventor proposes that it has~~ at least the following method steps are proposed:

- the at least one main computer transmits, with an N-th interrupt of a sequence of interrupts which are transmitted at a fixed time interval Δt, via the ATM bus a synchronization message (Sync) with a time indication (TOD), the time indication corresponding to the time of the main computer at the instant of the N-th interrupt plus the time interval Δt~~,~~;
- the at least one secondary computer reads, with good probability, the synchronization message via the ATM bus, sets its internal clock to the communicated time with the occurrence of the next interrupt and transmits, via the ATM bus, a success message (Ack) with an identifier of the secondary computer to the main computer~~,~~;
- the main computer reads the success message and decides, on the basis of the message propagation time, whether the success message was transmitted at the right time~~,~~;
- in the case of correctly timed transmission, the corresponding secondary computer is defined as synchronized~~,~~; and
- in the case of non-correctly timed transmission, the corresponding secondary computer is defined as unsynchronized.

In accordance with ~~a refinement~~ an alternative embodiment of the method according to the present invention, there may also occur between the interrupts outlined above further interrupts which are not taken into account in the method for time synchronization.

In accordance with the concept of the present invention, the main computer, with the (N + 2)-th interrupt, can again carry out time synchronization in accordance with the abovementioned method in order ~~that~~ for secondary computers that were possibly non-synchronized during the first scan through the time synchronization ~~are~~ to be synchronized ~~by means of~~ via the renewed performance of the time synchronization. Moreover, after a certain period of time has elapsed, differences in running of the individual hardware clocks of the individual computers of the computer network can give rise to a relative deviation in the timekeeping of the individual computers, thereby necessitating renewed synchronization.

It goes without saying that these time synchronizations can be repeated at specific predetermined intervals in order to keep the computer network permanently time-synchronized.

In accordance with the method according to the present invention, an identification mechanism for synchronized or non-synchronized computers can be established in the main computer, in which a specific secondary computer is deemed to be synchronized if the success message arrives at the main computer between the (N + 1)-th and the (N + 2)-th interrupt.

In this way, the main computer (in each case, without setting up any other particular connections to the secondary computers) can identify which secondary computers are in the synchronized state or in the non-synchronized state.

A typical magnitude of the time interval Δt at which the synchronization interrupts are transmitted is 23.5 msec. The typical accuracy of the time interval Δt is better than a few nsec, on which, however, the pure program run time, which lies in the region of a few μsec, is superposed.

A further ~~refinement~~ embodiment according to the present invention ~~of the presented method for time-synchronization consists in~~ involves further main computers being provided in the computer network~~,~~ which, in turn, have a superordinate computer, at least with regard to the system time, and are synchronized with one another according to the abovementioned method. This makes it possible for even a relatively large computer network ~~comprising~~ having, for example, a ~~plurality~~ number of clusters, each ~~comprising~~ including a main computer and a plurality of subordinate secondary computers, to be synchronized in such a way that ~~firstly~~ the main computers are first synchronized with regard to their system time and ~~the main computers~~ then in turn they independently synchronize, in accordance with the abovementioned method - their assigned secondary computers.

However, it should be pointed out that it is also possible, in a computer network in which all the computers are interconnected via an ATM bus, to define a single main computer which carries out the time synchronization via the ATM bus, so that all, that is to say all further main computers and all secondary computers, are synchronized with this time synchronization message. If a main computer which does not itself trigger the time synchronization wishes to identify whether its secondary computers assigned to it are now time-synchronized, then it is possible for it to monitor the ATM bus with regard to the success messages of the individual secondary computers and, accordingly, to decide whether or not the secondary computers assigned to it are time-synchronized.

Advantageously, the communicated time may also include the date and, in a particular embodiment, the ATM bus may be an AMX bus.

In addition to the method ~~according to~~ of the present invention, ~~the inventors~~ it is proposed, in accordance with a further concept of the present invention, ~~propose configuring~~ to configure a computer network known per se, preferably of a switching computer system, ~~comprising~~ including at least one main computer (Master) with, in each case, at least one assigned secondary computer (Slave), each computer being provided with at least one internal clock, and the

computers being connected via at least one ATM bus (ATM = asynchronous transfer mode), to the effect that:

- the at least one main computer is provided with ~~means~~ a transmitter which ~~transmit~~ transmits, with an N-th interrupt of a sequence of interrupts which are transmitted at a fixed time interval Δt, via the ATM bus a synchronization message (Sync) with a time indication (TOD), the time indication corresponding to the time of day of the main computer at the instant of the N-th interrupt plus the time interval Δt~~,~~;

- the at least one secondary computer is provided with ~~means~~ a part for reading the synchronization message via the ATM bus, its internal clock being set to the communicated time with the occurrence of the next interrupt, and has ~~means~~ a transmitter for transmitting a success message (Ack) with an identifier of the secondary computer to the main computer via the ATM bus~~,~~;

- the main computer has ~~means~~ a part for reading the success message and is provided with a decision ~~means~~ part which, on the basis of the message propagation time, ~~decide~~ decides whether the success message was transmitted at the right time~~,~~;

- in the main computer a memory ~~means being~~ is provided in which there is stored, in the case of correctly timed transmission, the definition of the corresponding secondary computer as synchronized~~,~~; and

- in the case of non-correctly timed transmission, the definition of the corresponding secondary computer as unsynchronized.

According to the present invention, there may also be provided, in addition to the interrupts provided for the time synchronization, further interrupts which are not taken into account during the time synchronization.

In a particular embodiment of the computer network, it may furthermore be provided that the ~~means of~~ the main computer ~~for time synchronization are provided with~~ include a repetition ~~means~~ function which, with the (N + 2)-th interrupt, again performs ~~a~~ the time synchronization. This is particularly important

if the time synchronization is intended to be maintained over a relatively long period of time.

In accordance with a particular embodiment ~~according to the invention~~ of the inventive computer network, it is proposed that the decision ~~means~~ part of the main computer defines a specific secondary computer as synchronized if the success message arrives at the main computer between the (N + 1)-th and the (N + 2)-th interrupt. A typical magnitude of the time interval between the interrupts may be specified as 23.5 msec.

In accordance with the method outlined above, further main computers may also be provided in the computer network, which, in turn, have a superordinate computer, at least with regard to the system time, and are synchronized with one another according to the abovementioned method.

Furthermore, it may be advantageous if the communicated time contains not only just the time of day but also the date.

In another ~~typical refinement~~ embodiment of the computer network ~~according to~~ of the present invention, the ATM bus may be an AMX bus.

~~Further refinements, additional features and advantages of the invention emerge from the following description of a preferred exemplary embodiment with reference to the drawings and from the subclaims.~~

~~It is understood that the features of the invention that have been mentioned above and those that have yet to be explained below can be used not only in the respectively specified combination but also in other combinations or by themselves, without departing from the scope of the invention.~~

~~The invention will be explained in more detail below, with reference to the drawing.~~

Additional features and advantages of the present invention are described in, and will be apparent from, the following Detailed Description of the Preferred Embodiments and the Drawings.

DESCRIPTION OF THE DRAWINGS

~~figure~~ Figure 1 ~~:~~ shows schematic illustration of a computer network; and

~~figure~~ Figure 2~~:~~ shows an illustration of the method sequence according to the present invention against the time axis.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 shows a schematic illustration of a computer network having four computers 1 to 4 illustrated by way of example. The computer 1 represents the main computer (Master) 1, which is provided with a processor (MP-Master = Main Processor Master) 1.1, a crystal-controlled clock (HW-Clock = Hardware Clock) 1.2 and an interface 1.3 to an AMX bus 5 via the ATM connecting line 1.4.

Also shown are the secondary computers 2 to 3, which are each likewise equipped with a processor 2.1 to 4.1, a clock 2.2 to 4.2 and an ATM interface 2.3 to 4.3. The secondary computers 2 to 4 are also, in each case, connected to the AMX bus 5 via an ATM connecting line 2.4 to 4.4.

The connecting arrows 6.1 to 6.3 are intended to illustrate that the time synchronization to be carried out acts on the secondary computers 2 to 4 in a manner proceeding from the main computer 1.

Figure 2 shows the time profile of the present invention's method for time synchronization, which can be carried out using the computer network from ~~figure~~ Figure 1. The time axis t is shown running from left to right. The four computers with their processors 1.1 to 4.1 are listed in a manner arranged from top to bottom. The time synchronization interrupts (ATM ticks) are specified in the topmost line along the time axis, ~~said~~ the interrupts having the interrupts N to N + 3 at a time interval Δt of 23.5 msec. With the first interrupt N, the main computer 1 sends a synchronization message with the current time TOD at the instant of the N-th interrupt plus 23.5 msec (TOD-S). This sent time TOD-S thus corresponds to the instant at which the (N + 1)-th interrupt occurs. In the time profile, the synchronization message (Sync) is read both at the secondary computer 2 and at the secondary computer 3. After receiving this synchronization message, the two computers 2 and 3 set their internal clocks 2.2 and 3.2 to the communicated time TOD-S with start beginning at the (N + 1)-th interrupt. In addition, after the (N + 1)-th interrupt, they send a success message (Ack) to the main computer 1

with the information that the synchronization message was received and the time on the internal clock was set correspondingly. However, the third secondary computer 4 receives the synchronization message only after the (N + 1)-th interrupt, with the result that it sets its internal clock to the communicated time only for the next interrupt; that is, ~~to say~~ for an interrupt that is too late. Consequently, its system time has an error of $\Delta t = 23.5$ msec. Accordingly, it also sends the success message to the main computer only after the (N + 2)-th interrupt.

Thus, between the (N - 1)-th and the (N + 2)-th interrupt, the main computer registers that the two secondary computers 2 and 3 have synchronized their internal clocks 2.2 and 3.2, in accordance with the synchronization message (Sync), while no success message (Ack) has yet been transmitted by the secondary computer 3. Consequently, the main computer knows that only the secondary computers 2 and 3 have been correctly synchronized with regard to their time setting, while the fate of the computer 3 remains open. Once the main computer receives the success message of the secondary computer 3 after the (N + 2)-th interrupt, the main computer knows that this computer was definitely not synchronized correctly. With the (N + 2)-th interrupt, ~~in other words~~ or in the case of the next even-numbered interrupt, the main computer once again sends a second group of synchronization messages with the current time at the instant of the (N + 2)-th interrupt plus 23.5 msec to the non-synchronized secondary computer 4 of the computer network and the synchronization of the secondary computer 4 with the subsequent signaling to the main computer starts from the beginning. In addition, the following cycles may be used to synchronize other as yet unsynchronized computers (not illustrated here).

If this method is repeated often enough, all the secondary computers are time-synchronized with the main computer. In this case, the inaccuracy of the time setting does not depend on the time profile of the message from the main computer to the secondary computer, but rather is merely dependent on the accuracy of the time interval Δt between the individual interrupts. Since the uncertainty of this time interval lies in the region of a few nsec, the time synchronization ~~by means of~~ via

the method described above is also extremely accurate and, thus, at any rate corresponds to the requirements of +/- 50 msec with regard to the communicated time of day including date.

If, in addition to the sent time of day, a time stamp (that is to say, a counter) is also sent with the synchronization message, the resolution of which time stamp is in the region of a few milliseconds, then the method described above also makes it possible to set the relative time stamp of the computers of the entire computer network with an accuracy lying in the region of the resolution of the time stamp.

Consequently, the method described satisfies the requirements with regard to the synchronization time (date/time of day: +/- 50 msec, relative time stamp: +/- 1 msec).

Although the present invention has been described with reference to specific embodiments, those of skill in the art will recognize that changes may be made thereto without departing from the spirit and scope of the invention as set forth in the hereafter appended claims.

~~Abstract~~

ABSTRACT OF THE DISCLOSURE

~~Method for the time synchronization of a computer network, and computer network with time synchronization~~

~~The invention relates to a~~ A method for ~~the~~ time synchronization of a computer network by a main computer, in which case, for synchronization with an N-th interrupt, a time signal corresponding to the instant of the interrupt plus a time interval between the interrupts is transmitted on an ATM bus and the secondary computers to be synchronized set their clock to this transmitted time signal with the next

Description

Method for the time synchronization of a computer network, and computer network with time synchronization

The invention relates to a method for the time synchronization of a computer network, preferably of a switching computer system, comprising at least one main computer (Master) with in each case at least one assigned secondary computer (slave), each computer being provided with at least one internal clock, and the computers being connected via at least one ATM bus (ATM = asynchronous transfer mode).

Furthermore, the invention relates to a computer network, preferably a switching computer system, comprising at least one main computer (Master) with in each case at least one assigned secondary computer (Slave), each computer being provided with at least one internal clock, and the computers being interconnected via at least one ATM bus.

At present there is no known prior art for real-time process computer systems, in particular switching computer systems, in which time synchronization of the participating computers in the computer network is realized with an accuracy with regard to date and time of day of at least +/- 50 msec and a relative time stamp of at least +/- 1 msec. The currently used switching computer systems, such as, for example, the applicant's switching computer system EWSD or EWSX, are realized either as mono-processor systems or strictly coupled multi-processor systems. With this type of configuration, particular time synchronization is inherently given on account of the strict coupling of the processors, or of the just one processor that is present.

In the course of general development, however, distributed real-time process computer systems are also intended to be used as switching computer systems. The requirement for charge registration means that it is necessary for the process computers situated in the process computer system to be provided with a synchronized time, with regard to date and time of day, which has a maximum error of +/- 50 msec. This requirement is substantiated by the charge registration since the charge registration creates tickets with a time indication at all the computer components of the distributed system. Furthermore, it is necessary, on account of the internal data transport protocol of the distributed system, to achieve a relative time stamp - that is to say a counter - with an accuracy of at least +/- 1 msec for all the computers in the network system. The relative resolution of such a time stamp, that is to say the time spacing from one counter to the next counter, typically lies in a range of about 10 msec. The time stamp is required in order to measure message throughput times in the system, in order to analyze incorrect behavior or to carry out performance analyses in the distributed system, with the aid of system tracers. In order that the events from the trace results can be correctly assigned with respect to time, a system-wide synchronized time of day, that is to say a correspondingly exact time stamp, is likewise required.

It is an object of the invention, therefore, to present a method for the time synchronization of a computer network, preferably of a switching computer system, and a corresponding computer network, preferably a corresponding switching computer system, which achieves time synchronization for date/time of day of at least +/- 50 msec and for a general relative time stamp of at least +/- 1 msec, no direct connection between the individual computers, but rather only the ATM bus being utilized.

This object is achieved by means of the features of the respective first method claim and of the first apparatus claim.

With regard to the invention's method for the time synchronization of a computer network, preferably of a switching computer system, comprising at least one main computer (Master) and in each case at least one assigned secondary computer (Slave), each computer being provided with at least one internal clock, and the computers being connected via at least one ATM bus (ATM = asynchronous transfer mode), the inventor proposes that it has at least the following method steps:

- the at least one main computer transmits, with an N-th interrupt of a sequence of interrupts which are transmitted at a fixed time interval Δt, via the ATM bus a synchronization message (Sync) with a time indication (TOD), the time indication corresponding to the time of the main computer at the instant of the N-th interrupt plus the time interval Δt,

- the at least one secondary computer reads, with good probability, the synchronization message via the ATM bus, sets its internal clock to the communicated time with the occurrence of the next interrupt and transmits via the ATM bus a success message (Ack) with an identifier of the secondary computer to the main computer,

- the main computer reads the success message and decides, on the basis of the message propagation time, whether the success message was transmitted at the right time,

- in the case of correctly timed transmission, the corresponding secondary computer is defined as synchronized, and

- in the case of non-correctly timed transmission, the corresponding secondary computer is defined as unsynchronized.

In accordance with a refinement of the method according to the invention, there may also occur between the interrupts

outlined above further interrupts which are not taken into account in the method for time synchronization.

In accordance with the concept of the invention, the main computer, with the (N + 2)-th interrupt, can again carry out time synchronization in accordance with the abovementioned method in order that secondary computers that were possibly non-synchronized during the first scan through the time synchronization are synchronized by means of the renewed performance of the time synchronization. Moreover, after a certain period of time has elapsed, differences in running of the individual hardware clocks of the individual computers of the computer network can give rise to a relative deviation in the timekeeping of the individual computers, thereby necessitating renewed synchronization.

It goes without saying that these time synchronizations can be repeated at specific predetermined intervals in order to keep the computer network permanently time-synchronized.

In accordance with the method according to the invention, an identification mechanism for synchronized or non-synchronized computers can be established in the main computer, in which a specific secondary computer is deemed to be synchronized if the success message arrives at the main computer between the (N + 1)-th and the (N + 2)-th interrupt.

In this way, the main computer - in each case without setting up any other particular connections to the secondary computers - can identify which secondary computers are in the synchronized state or in the non-synchronized state.

A typical magnitude of the time interval Δt at which the synchronization interrupts are transmitted is 23.5 msec. The typical accuracy of the time interval Δt is

better than a few nsec, on which, however, the pure program run time, which lies in the region of a few µsec, is superposed.

A further refinement according to the invention of the presented method for time synchronization consists in further main computers being provided in the computer network, which in turn have a superordinate computer, at least with regard to the system time, and are synchronized with one another according to the abovementioned method. This makes it possible for even a relatively large computer network comprising, for example, a plurality of clusters, each comprising a main computer and a plurality of subordinate secondary computers, to be synchronized in such a way that firstly the main computers are synchronized with regard to their system time and the main computers in turn independently synchronize - in accordance with the abovementioned method - their assigned secondary computers.

However, it should be pointed out that it is also possible, in a computer network in which all the computers are interconnected via an ATM bus, to define a single main computer which carries out the time synchronization via the ATM bus, so that all, that is to say all further main computers and all secondary computers, are synchronized with this time synchronization message. If a main computer which does not itself trigger the time synchronization wishes to identify whether its secondary computers assigned to it are now time-synchronized, then it is possible for it to monitor the ATM bus with regard to the success messages of the individual secondary computers and accordingly to decide whether or not the secondary computers assigned to it are time-synchronized.

Advantageously, the communicated time may also include the date and, in a particular embodiment, the ATM bus may be an AMX bus.

In addition to the method according to the invention, the inventors, in accordance with a further concept of the invention, propose configuring a computer network known per se, preferably of a switching computer system, comprising at least one main computer (Master) with in each case at least one assigned secondary computer (Slave), each computer being provided with at least one internal clock, and the computers being connected via at least one ATM bus (ATM = asynchronous transfer mode), to the effect that

- the at least one main computer is provided with means which transmit, with an N-th interrupt of a sequence of interrupts which are transmitted at a fixed time interval Δt, via the ATM bus a synchronization message (Sync) with a time indication (TOD), the time indication corresponding to the time of day of the main computer at the instant of the N-th interrupt plus the time interval Δt,

- the at least one secondary computer is provided with means for reading the synchronization message via the ATM bus, its internal clock being set to the communicated time with the occurrence of the next interrupt, and has means for transmitting a success message (Ack) with an identifier of the secondary computer to the main computer via the ATM bus,

- the main computer has means for reading the success message and is provided with decision means which, on the basis of the message propagation time, decide whether the success message was transmitted at the right time,

- in the main computer a memory means being provided in which there is stored, in the case of correctly timed transmission, the definition of the corresponding secondary computer as synchronized, and

- in the case of non-correctly timed transmission, the definition of the corresponding secondary computer as unsynchronized.

According to the invention, there may also be provided, in addition to the interrupts provided for the time synchronization,

further interrupts which are not taken into account during the time synchronization.

In a particular embodiment of the computer network, it may furthermore be provided that the means of the main computer for time synchronization are provided with a repetition means which, with the (N + 2)-th interrupt, again performs a time synchronization. This is particularly important if the time synchronization is intended to be maintained over a relatively long period of time.

In accordance with a particular embodiment according to the invention of the computer network, it is proposed that the decision means of the main computer defines a specific secondary computer as synchronized if the success message arrives at the main computer between the (N + 1)-th and the (N + 2)-th interrupt. A typical magnitude of the time interval between the interrupts may be specified as 23.5 msec.

In accordance with the method outlined above, further main computers may also be provided in the computer network, which in turn have a superordinate computer, at least with regard to the system time, and are synchronized with one another according to the abovementioned method.

Furthermore, it may be advantageous if the communicated time contains not only just the time of day but also the date.

In another typical refinement of the computer network according to the invention, the ATM bus may be an AMX bus.

Further refinements, additional features and advantages of the invention emerge from the following description

of a preferred exemplary embodiment with reference to the drawings and from the subclaims.

It is understood that the features of the invention that have been mentioned above and those that have yet to be explained below can be used not only in the respectively specified combination but also in other combinations or by themselves, without departing from the scope of the invention.

The invention will be explained in more detail below, with reference to the drawing.

figure 1: schematic illustration of a computer network;

figure 2: illustration of the method sequence according to the invention against the time axis.

Figure 1 shows a schematic illustration of a computer network having four computers 1 to 4 illustrated by way of example. The computer 1 represents the main computer (Master) 1, which is provided with a processor (MP-Master = Main Processor Master) 1.1, a crystal-controlled clock (HW-Clock = Hardware Clock) 1.2 and an interface 1.3 to an AMX bus 5 via the ATM connecting line 1.4.

Also shown are the secondary computers 2 to 3, which are each likewise equipped with a processor 2.1 to 4.1, a clock 2.2 to 4.2 and an ATM interface 2.3 to 4.3. The secondary computers 2 to 4 are also in each case connected to the AMX bus 5 via an ATM connecting line 2.4 to 4.4.

The connecting arrows 6.1 to 6.3 are intended to illustrate that the time synchronization to be carried out acts on the secondary computers 2 to 4 in a manner proceeding from the main computer 1.

Figure 2 shows the time profile of the invention's method for time synchronization, which can be

carried out using the computer network from figure 1. The time axis t is shown running from left to right. The four computers with their processors 1.1 to 4.1 are listed in a manner arranged from top to bottom. The time synchronization interrupts (ATM ticks) are specified in the topmost line along the time axis, said interrupts having the interrupts N to N + 3 at a time interval Δt of 23.5 msec. With the first interrupt N, the main computer 1 sends a synchronization message with the current time TOD at the instant of the N-th interrupt plus 23.5 msec (TOD-S). This sent time TOD-S thus corresponds to the instant at which the (N + 1)-th interrupt occurs. In the time profile, the synchronization message (Sync) is read both at the secondary computer 2 and at the secondary computer 3. After receiving this synchronization message, the two computers 2 and 3 set their internal clocks 2.2 and 3.2 to the communicated time TOD-S with start beginning at the (N + 1)-th interrupt. In addition, after the (N + 1)-th interrupt, they send a success message (Ack) to the main computer 1 with the information that the synchronization message was received and the time on the internal clock was set correspondingly. However, the third secondary computer 4 receives the synchronization message only after the (N + 1)-th interrupt, with the result that it sets its internal clock to the communicated time only for the next interrupt - that is to say for an interrupt that is too late. Consequently, its system time has an error of Δt = 23.5 msec. Accordingly, it also sends the success message to the main computer only after the (N + 2)-th interrupt.

Thus, between the (N - 1)-th and the (N + 2)-th interrupt, the main computer registers that the two secondary computers 2 and 3 have synchronized their internal clocks 2.2 and 3.2, in accordance with the synchronization message (Sync), while no success message (Ack) has yet been transmitted by the secondary

computer 3. Consequently, the main computer knows that only the

secondary computers 2 and 3 have been correctly synchronized with regard to their time setting, while the fate of the computer 3 remains open. Once the main computer receives the success message of the secondary computer 3 after the (N + 2)-th interrupt, the main computer knows that this computer was definitely not synchronized correctly. With the (N + 2)-th interrupt - in other words in the case of the next even-numbered interrupt - the main computer once again sends a second group of synchronization messages with the current time at the instant of the (N + 2)-th interrupt plus 23.5 msec to the non-synchronized secondary computer 4 of the computer network and the synchronization of the secondary computer 4 with the subsequent signaling to the main computer starts from the beginning. In addition, the following cycles may be used to synchronize other as yet unsynchronized computers (not illustrated here).

If this method is repeated often enough, all the secondary computers are time-synchronized with the main computer. In this case, the inaccuracy of the time setting does not depend on the time profile of the message from the main computer to the secondary computer, but rather is merely dependent on the accuracy of the time interval Δt between the individual interrupts. Since the uncertainty of this time interval lies in the region of a few nsec, the time synchronization by means of the method described above is also extremely accurate and thus at any rate corresponds to the requirements of +/- 50 msec with regard to the communicated time of day including date.

If, in addition to the sent time of day, a time stamp (that is to say a counter) is also sent with the synchronization message, the resolution of which time stamp is in the region of a few milliseconds, then the method described above also makes it possible to set the relative time stamp of the computers of the entire computer network with

an accuracy lying in the region of the resolution of the time stamp.

Consequently, the method described satisfies the requirements with regard to the synchronization time (date/time of day: +/- 50 msec, relative time stamp: +/- 1 msec).

Patent Claims

1. A method for the time synchronization of a computer network, preferably of a switching computer system, comprising at least one main computer (Master) (1) with in each case at least one assigned secondary computer (Slave) (2, 3, 4), each computer (1, 2, 3, 4) being provided with at least one internal clock (1.2, 2.2, 3.2, 4.2), and the computers (1, 2, 3, 4) being connected via at least one ATM bus (5) (ATM = asynchronous transfer mode), characterized by the following method steps:

- the at least one main computer (1) transmits, with an N-th interrupt of a sequence of interrupts which are transmitted at a fixed time interval Δt, via the ATM bus (5) a synchronization message (Sync) with a time indication (TOD-S) and, if appropriate, a time stamp (value of a counter), the time indication corresponding to the time of day (TOD) of the main computer at the instant of the N-th interrupt plus the time interval Δt,

- the at least one secondary computer (2, 3, 4) reads, with good probability, the synchronization message (Sync) via the ATM bus (5), sets its internal clock (2.2, 3.2, 4.2) to the communicated time (TOD-S) with the occurrence of the next interrupt and transmits via the ATM bus (5) a success message (Ack) with an identifier of the secondary computer (2, 3, 4) to the main computer (1),

- the main computer (1) reads the success message (Ack) and decides, on the basis of the message propagation time, whether the success message (Ack) was transmitted at the right time,

- in the case of correctly timed transmission, the corresponding secondary computer is defined as synchronized, and

- in the case of non-correctly timed transmission, the corresponding secondary computer is defined as unsynchronized.

2. The method as claimed in claim 1, characterized in that, between the interrupts in accordance with claim 1, further

interrupts can occur which are not taken into account in the method.

3. The method as claimed in one of the preceding claims, characterized in that the main computer (1), with the (N + 2)-th interrupt, again performs a time synchronization in accordance with claim 1.

4. The method as claimed in one of the preceding claims, characterized in that a specific secondary computer (2, 3, 4) is deemed to be synchronized if the success message (Ack) arrives at the main computer (1) between the (N + 1)-th and the (N + 2)-th interrupt.

5. The method as claimed in one of the preceding claims, characterized in that the time interval Δt is 23.5 msec.

6. The method as claimed in one of the preceding claims, characterized in that further main computers are provided in the computer network, which in turn have a superordinate computer, at least with regard to the system time, and are synchronized with one another according to the abovementioned method.

7. The method as claimed in one of the preceding claims, characterized in that the communicated time (TOD-S) also contains the date.

8. The method as claimed in one of the preceding claims, characterized in that the ATM bus is an AMX bus.

9. A computer network, preferably of a switching computer system, comprising at least one main computer (Master) (1) with in each case at least one assigned secondary computer (Slave) (2, 3, 4), each computer (1, 2, 3, 4) being provided with at least one internal clock (1.2,

2.2, 3.2, 4.2), and the computers (1, 2, 3, 4) being connected via at least one ATM bus (5) (ATM = asynchronous transfer mode), characterized in that

- the at least one main computer (1) is provided with means which transmit, with an N-th interrupt of a sequence of interrupts which are transmitted at a fixed time interval Δt, via the ATM bus (5) a synchronization message (Sync) with a time indication (TOD-S) and, if appropriate, a time stamp (value of a counter), the time indication corresponding to the time of day (TOD) of the main computer at the instant of the N-th interrupt plus the time interval Δt,

- the at least one secondary computer (2, 3, 4) is provided with means for reading the synchronization message (Sync) via the ATM bus (5), its internal clock (2.2, 3.2, 4.2) being set to the communicated time (TOD-S) with the occurrence of the next interrupt, and has means for transmitting a success message (Ack) with an identifier of the secondary computer (2, 3, 4) to the main computer (1) via the ATM bus (5),

- the main computer (1) has means for reading the success message (Ack) and is provided with decision means which, on the basis of the message propagation time, decide whether the success message (Ack) was transmitted at the right time,

- in the main computer (1) a memory means being provided in which there is stored, in the case of correctly timed transmission, the definition of the corresponding secondary computer as synchronized, and

- in the case of non-correctly timed transmission, the definition of the corresponding secondary computer as unsynchronized.

10. The computer network as claimed in claim 9, characterized in that, between the interrupts in accordance with claim 1, further interrupts are

provided which are not taken into account during the time synchronization.

11. The computer network as claimed in one of the preceding claims 9 - 10, characterized in that the means of the main computer (1) for time synchronization are provided with a repetition means which, with the (N + 2)-th interrupt, again performs a time synchronization.

12. The computer network as claimed in one of the preceding claims 9 - 11, characterized in that the decision means of the main computer (1) defines a specific secondary computer (2, 3, 4) as synchronized if the success message (Ack) arrives at the main computer (1) between the (N + 1)-th and the (N + 2)-th interrupt.

13. The computer network as claimed in one of the preceding claims 9 - 12, characterized in that the time interval Δt is 23.5 msec.

14. The computer network as claimed in one of the preceding claims 9 - 13, characterized in that further main computers are provided in the computer network, which in turn have a superordinate computer, at least with regard to the system time, and are synchronized with one another according to the abovementioned method.

15. The computer network as claimed in one of the preceding claims 9 - 14, characterized in that the communicated time also contains the date.

16. The computer network as claimed in one of the preceding claims 9 - 15, characterized in that the ATM bus is an AMX bus.

GR 99 P 1069

Abstract

Method for the time synchronization of a computer network, and computer network with time synchronization

The invention relates to a method for the time synchronization of a computer network by a main computer, in which case, for synchronization with an N-th interrupt, a time signal corresponding to the instant of the interrupt plus a time interval between the interrupts is transmitted on an ATM bus and the secondary computers to be synchronized set their clock to this transmitted time signal with the next interrupt.

Declaration and Power of Attorney For Patent Application
Erklärung Für Patentanmeldungen Mit Vollmacht
German Language Declaration

Als nachstehend benannter Erfinder erkläre ich hiermit an Eides Statt:

dass mein Wohnsitz, meine Postanschrift, und meine Staatsangehörigkeit den im Nachstehenden nach meinem Namen aufgeführten Angaben entsprechen,

dass ich, nach bestem Wissen der ursprüngliche, erste und alleinige Erfinder (falls nachstehend nur ein Name angegeben ist) oder ein ursprünglicher, erster und Miterfinder (falls nachstehend mehrere Namen aufgeführt sind) des Gegenstandes bin, für den dieser Antrag gestellt wird und für den ein Patent beantragt wird für die Erfindung mit dem Titel:

Verfahren zur Zeitsynchronisation eines Computerverbundes und Computerverbund mit Zeitsynchronisation

deren Beschreibung

(zutreffendes ankreuzen)
☐ hier beigefügt ist.
☒ am 14.01.2000 als
PCT internationale Anmeldung
PCT Anmeldungsnummer PCT/EP00/00326
eingereicht wurde und am _____
abgeändert wurde (falls tatsächlich abgeändert).

Ich bestätige hiermit, dass ich den Inhalt der obigen Patentanmeldung einschliesslich der Ansprüche durchgesehen und verstanden habe, die eventuell durch einen Zusatzantrag wie oben erwähnt abgeändert wurde.

Ich erkenne meine Pflicht zur Offenbarung irgendwelcher Informationen, die für die Prüfung der vorliegenden Anmeldung in Einklang mit Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) von Wichtigkeit sind, an.

Ich beanspruche hiermit ausländische Prioritätsvorteile gemäss Abschnitt 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 119 aller unten angegebenen Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde, und habe auch alle Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde nachstehend gekennzeichnet, die ein Anmeldedatum haben, das vor dem Anmeldedatum der Anmeldung liegt, für die Priorität beansprucht wird.

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Method for the time synchronisation of a computer network and computer network with time synchronisation

the specification of which

(check one)
☐ is attached hereto.
☒ was filed on 14.01.2000 as
PCT international application
PCT Application No. PCT/EP00/00326
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

German Language Declaration

Prior foreign appplications Priorität beansprucht			Priority Claimed
99100899.6 (Number) (Nummer)	EP (Country) (Land)	19.01.1999 (Day Month Year Filed) (Tag Monat Jahr eingereicht)	☒ Yes Ja ☐ No Nein
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	☐ Yes Ja ☐ No Nein
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	☐ Yes Ja ☐ No Nein

Ich beanspruche hiermit gemäss Absatz 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 120, den Vorzug aller unten aufgeführten Anmeldungen und falls der Gegenstand aus jedem Anspruch dieser Anmeldung nicht in einer früheren amerikanischen Patentanmeldung laut dem ersten Paragraphen des Absatzes 35 der Zivilprozeßordnung der Vereinigten Staaten, Paragraph 122 offenbart ist, erkenne ich gemäss Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) meine Pflicht zur Offenbarung von Informationen an, die zwischen dem Anmeldedatum der früheren Anmeldung und dem nationalen oder PCT internationalen Anmeldedatum dieser Anmeldung bekannt geworden sind.

I hereby claim the benefit under Title 35. United States Code. §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §122, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occured between the filing date of the prior application and the national or PCT international filing date of this application.

PCT/EP00/00326 (Application Serial No.) (Anmeldeseriennummer)	14.01.2000 (Filing Date D, M, Y) (Anmeldedatum T, M, J)	anhängig (Status) (patentiert, anhängig, aufgegeben)	pending (Status) (patented, pending, abandoned)
(Application Serial No.) (Anmeldeseriennummer)	(Filing Date D,M,Y) (Anmeldedatum T, M; J)	(Status) (patentiert, anhängig, aufgeben)	(Status) (patented, pending, abandoned)

Ich erkläre hiermit, dass alle von mir in der vorliegenden Erklärung gemachten Angaben nach meinem besten Wissen und Gewissen der vollen Wahrheit entsprechen, und dass ich diese eidesstattliche Erklärung in Kenntnis dessen abgebe, dass wissentlich und vorsätzlich falsche Angaben gemäss Paragraph 1001, Absatz 18 der Zivilprozessordnung der Vereinigten Staaten von Amerika mit Geldstrafe belegt und/oder Gefängnis bestraft werden koennen, und dass derartig wissentlich und vorsätzlich falsche Angaben die Gültigkeit der vorliegenden Patentanmeldung oder eines darauf erteilten Patentes gefährden können.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

German Language Declaration

VERTRETUNGSVOLLMACHT: Als benannter Erfinder beauftrage ich hiermit den nachstehend benannten Patentanwalt (oder die nachstehend benannten Patentanwälte) und/oder Patent-Agenten mit der Verfolgung der vorliegenden Patentanmeldung sowie mit der Abwicklung aller damit verbundenen Geschäfte vor dem Patent- und Warenzeichenamt: *(Name und Registrationsnummer anführen)*

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

And I hereby appoint

Customer No.

Telefongespräche bitte richten an: *(Name und Telefonnummer)*

Direct Telephone Calls to: *(name and telephone number)*

Ext. _____

Postanschrift:

Send Correspondence to:

Bell, Boyd & Lloyd LLC
Three First National Plaza, 70 West Madison Street, Suite 3300 60602-4207 Chicago, Illinois
Telephone: (001) 312 372 11 21 and Facsimile (001) 312 372 20 98
or
Customer No.

Voller Name des einzigen oder ursprünglichen Erfinders:	Full name of sole or first inventor:
Dr. HARALD EGGERS 1-CD	Dr. HARALD EGGERS
Unterschrift des Erfinders / Datum: H. Eggs 4.7.01	~~Inventor's signature~~ / Date: Harald Eggs 4.7.01
Wohnsitz: VIERKIRCHEN, DEUTSCHLAND	Residence: VIERKIRCHEN, GERMANY DEX
Staatsangehörigkeit: DE	Citizenship: DE
Postanschrift: HERBSTSTR. 1 85256 VIERKIRCHEN	Post Office Addess: HERBSTSTR. 1 85256 VIERKIRCHEN
Voller Name des zweiten Miterfinders (falls zutreffend): JUERGEN SCHUCHT 2-CD	Full name of second joint inventor, if any: JUERGEN SCHUCHT
Unterschrift des Erfinders / Datum: J Schucht 11.7.01	~~Second Inventor's signature~~ / Date: Jürgen Schucht 11.7.01
Wohnsitz: MUENCHEN, DEUTSCHLAND	Residence: MUENCHEN, GERMANY DEX
Staatsangehörigkeit: DE	Citizenship: DE
Postanschrift: HOFMANNSTR. 36 A 81379 MUENCHEN	Post Office Address: HOFMANNSTR. 36 A 81379 MUENCHEN

(Bitte entsprechende Informationen und Unterschriften im Falle von dritten und weiteren Miterfindern angeben).

(Supply similar information and signature for third and subsequent joint inventors).

Voller Name des dritten Miterfinders:	Full name of third joint inventor:
RICHARD STURM	RICHARD STURM
~~Unterschrift des Erfinders~~ Datum Richard Sturm 19.07.01	Inventor's signature Date
Wohnsitz ROSENHEIM, DEUTSCHLAND DE	Residence ROSENHEIM, GERMANY
~~Staatsangehörigkeit~~ DE	Citizenship DE
Postanschrift ILLERSTR.8 83026 ROSENHEIM	Post Office Address ILLERSTR.8 83026 ROSENHEIM
Voller Name des vierten Miterfinders:	Full name of fourth joint inventor:
Unterschrift des Erfinders Datum	Inventor's signature Date
Wohnsitz ,	Residence ,
Staatsangehörigkeit	Citizenship
Postanschrift	Post Office Address
Voller Name des fünften Miterfinders:	Full name of fifth joint inventor:
Unterschrift des Erfinders Datum	Inventor's signature Date
Wohnsitz ,	Residence ,
Staatsangehörigkeit	Citizenship
Postanschrift	Post Office Address
Voller Name des sechsten Miterfinders:	Full name of sixth joint inventor:
Unterschrift des Erfinders Datum	Inventor's signature Date
Wohnsitz ,	Residence ,
Staatsangehörigkeit	Citizenship
Postanschrift	Post Office Address

(Bitte entsprechende Informationen und Unterschriften im Falle von dritten und weiteren Miterfindern angeben).

(Supply similar information and signature for third and subsequent joint inventors).